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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,849	03/30/2004	Seong Cheol Kang	LT-0051	2338

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EXAMINER	
BROWN, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,849	KANG, SEONG CHEOL	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 8 is objected to because of the following informalities: On line 5 of claim 8 "occurance" should be spelled "occurrence". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Atkinson(US Patent 6,802,015).

As to claim 1, Atkinson discloses a method for controlling CPU(CPU 112, see Fig. 1) speed transition, comprising receiving a System Management Interrupt (SMI) signal(see column 7, line 27), determining whether a bus master device(PCI bus 124, see Fig. 1) is in an active state when the SMI signal is for performing CPU speed transition(see column 7, lines 58-62), and canceling the CPU speed transition operation when the bus master device is in the active state and generating at prescribed intervals a retry SMI signal(see column 9, lines 5-7).

As to claim 2, Atkinson discloses the method of comprising performing the CPU speed transition operation when the bus master device is not in the active state(see column 7, lines 28-41).

As to claim 3, Atkinson discloses the method wherein the retry SMI signal generated at prescribed intervals is one of a watchdog timer SMI signal and an embedded control SMI signal to retry the CPU speed transition operation(see column 7, lines 28-31).

As to claim 4, Atkinson discloses the method wherein the determining comprises disabling occurrences of additional watchdog timer SMI signals when the received SMI signal is the watchdog timer SMI signal to retry the CPU transition operation; and re-determining whether the bus master device is in the active state(see column 7, lines 58-62).

As to claim 5, Atkinson discloses the method wherein the determining comprises disabling occurrence of additional embedded controller SMI signals when the received SMI signal is an embedded controller SMI signal to retry the CPU speed transition operation; and re-determining whether the bus master device is in the active state(see column 7, lines 58-62).

As to claim 6, Atkinson discloses the method wherein the determining comprises performing a prescribed operation corresponding to the received SMI signal when the received SMI signal is not an SMI signal for CPU speed transition, the watchdog timer SMI signal to retry the CPU speed transition operation or the embedded controller SMI to retry the CPU speed transition operation(see column 7, lines 58-62).

As to claim 7, Atkinson discloses the method wherein the SMI signals are at least one of a hardware generated signal and an application program generated signal(see column 7, lines 58-62).

As to claim 8, Atkinson discloses a portable computer(laptop computer system 100, see Fig. 1), comprising a CPU(CPU 112, see Fig. 1) configured to operate using at least two speeds(multiple frequencies(see column 11, line 21), a controller(speed control algorithm 185, see Fig. 1) configured to perform a prescribed operation to transition between the at least two speeds of the CPU, and an interrupt occurrence reason recognition means(keyboard controller 160, see Fig. 1) for recognizing an occurrence reason of an interrupt signal(see column 8, line 67- column 9, line 1). Atkinson also discloses an active state checking means(Real Time Clock(RTC), column 7, line 32) for checking an active state of a predetermined device(PCI bus 124, see Fig. 1), and interrupt generating means(South Bridge 168, see Fig. 1) for creating a second interrupt signal to retry the prescribed operation for the CPU speed transition when the interrupt occurrence reason recognition means determines that a first interrupt signal is created for the CPU speed transition and the active state checking means determines that the predetermined device is in the active state.

As to claim 9, Atkinson discloses the portable computer wherein the interrupt signal for the CPU speed transition is responsive to a change of CPU use amount, switching between AC adapter and battery power sources, reduction of battery lifetime, runtime setup of a user and temperature variation(see column 11, lines 44-47).

As to claim 10, Atkinson discloses the portable computer wherein the interrupt generating means creates the second interrupt signal using a predetermined timer contained in the system(see column 7, lines 62-67).

As to claim 11, Atkinson discloses the portable computer wherein the predetermined timer contained in the system is a watchdog timer or an inner timer of an embedded controller(see column 7, lines 28-31).

As to claim 12, Atkinson discloses the portable computer wherein the second interrupt signal is created at intervals of a predetermined time determined by a system BIOS(see column 11, lines 52-54).

As to claim 13, Atkinson discloses the portable computer wherein the predetermined device is a bus master device(PCI bus 124, see Fig. 1).

As to claim 14, Atkinson discloses the portable computer wherein the second interrupt is repeatedly generated until the CPU transition is performed(see column 11, lines 52-65), and wherein the portable computer is a notebook computer(laptop computer system 100, see Fig. 1).

As to claim 15, Atkinson discloses an apparatus, comprising an interrupt receiver(Keyboard controller 160, see Fig. 1) configured to receive interrupt signals, and an interrupt generator(South Bridge 168, see Fig. 1) coupled to the interrupt receiver and configured to generate a second interrupt signal to retry a prescribed operation needed for CPU speed transition when a first interrupt signal for the CPU speed transition is received and a bus master device(PCI bus 124, see Fig. 1) is in an active state.

As to claim 16, Atkinson discloses the apparatus wherein the interrupt generator creates the second interrupt signal using a predetermined timer contained in the system(see column 7, lines 62-67).

As to claim 17, Atkinson discloses the apparatus wherein the predetermined timer contained in the system is at least one of a watchdog timer and an inner timer of an embedded controller(see column 7, lines 28-31).

As to claim 18, Atkinson discloses the apparatus wherein the second interrupt signal is created at intervals of a predetermined time determined by a system BIOS(see column 11, lines 52-54).

As to claim 19, Atkinson discloses the apparatus wherein the apparatus is in a notebook computer(laptop computer system 100, see Fig. 1).

As to claim 20, Atkinson discloses the apparatus wherein the interrupt signals are one of hardware interrupts and software interrupts(see column 7, lines 28-31).

As to claim 21, Atkinson discloses an article including a machine-readable storage medium(BIOS ROM 144, see Fig. 1) containing instructions for controlling CPU(CPU 112, see Fig. 1) speed transition in a computer system(laptop computer system 100, see Fig. 1), said instructions, when executed in the computer system, causing the computer system to receive an System Management Interrupt (SMI) signal(see column 7, line 27), determine whether a bus master device(PCI bus 124, see Fig. 1) is in an active state when the SMI signal is a first SMI CPU speed transition signal(see column 7, lines 58-62), and cancel the CPU speed transition operation when

the bus master device is in the active state and generate at predetermined intervals an event(see column 9, lines 5-7).

As to claim 22, Atkinson discloses the article wherein the event is a second SMI CPU speed transition signal(see column 9, lines 5-7).

As to claim 23, Atkinson discloses the article wherein the event is one of a hardware interrupt and a software interrupt(see column 7, lines 28-31).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Brown whose telephone number is (571)272-5932. The examiner can normally be reached on Monday-Thursday from 7:00am to 5:30pm(EST).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIRS) system. Status information for the published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications are available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 886-217-9197 (toll-free).

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